CLAIMS:

1. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items.

2. A data processing apparatus comprising an array of processing elements, which are operable to process respective data items in accordance with a common received instruction, wherein the processing elements are operably divided into a plurality of processing blocks having at least one processing element, the processing blocks being operable to process respective groups of data items.

3. An apparatus as claimed in claim 1 or 2, wherein at least one of the processing blocks is a redundant block operable to process a group of data items in place of a faulty processing block.

4. An apparatus as claimed in claim 3, comprising fault detection means operable to detect a fault occurring in a processing block and to transfer the data processing function of that processing block to a redundant processing block.

5. An apparatus as claimed in any one of the preceding claims, wherein each processing block is provided with at least one redundant processing element operable to process data items in place of a faulty processing element of the block concerned.

6. An apparatus as claimed in claim 5, wherein the processing elements of a processing block are arranged in groups having a predetermined number of processing elements therein, each such group containing at least one such redundant processing element for replacing a faulty processing element in the group.

7. An apparatus as claimed in claim 5 or 6, comprising fault detection means operable to detect a fault occurring in a processing element and to transfer the data processing function of that processing element to a redundant processing element.

8. An apparatus as claimed in any one of the preceding claims, wherein each processing block includes a mathematical expression evaluator which is operable evaluate a mathematical expression for each processing element and to provide respective evaluations to the processing elements in the processing block.

9. An apparatus as claimed in claim 8, wherein the

expression evaluator is operable to evaluate the expression ax+by+c for each processing element in the block, each processing element being assigned a specific (x, y) value and a, b and c being coefficients supplied to the expression evaluator.

10. An apparatus as claimed in claim 9, wherein the coefficients a, b and c are supplied to the expression evaluator by the processing elements of the processing block.

11. An apparatus as claimed in claim 9, wherein the coefficients a, b and c are supplied to the expression evaluator by a source external to the processing block.

12. An apparatus as claimed in any one of the preceding claims, wherein instructions and data items to be processed by the processing elements are supplied separately from one another to the processing elements.

13. An apparatus as claimed in any one of the preceding claims, wherein the data items to be processed by processing elements in a processing block are supplied by processing elements in that processing block.

14. An apparatus as claimed in any one of the preceding claims, wherein each processing element

comprises a processing unit for receiving data items and instruction items, which processing unit is operable to process the data items according to received instruction items, a memory unit for storing data items received from the processing unit, and a register file arranged between the processor unit and the memory unit, which register file is operable to store data items from the processor unit and from the memory unit, for transfer to the other of those units and is operable to store data items for processing by the processor unit of the processing element.

15. A data processing apparatus as claimed in any one of the preceding claims comprising an external memory for storing data items and instruction items; and

a controller means for controlling transfer of data and instruction items between each processing element and the external memory,

wherein the or each processing element comprises:

a processor unit connected to receive data items and instruction items and operable to process the said data items in accordance with the said instruction items;

a plurality of storage registers for temporarily

storing data items for input to the processor unit, at least one of the storage registers being operable to store an offset value;

a memory unit for storing data items and address data indicating an external memory address; and

a register file for storing data items, the register file being connected between the processor unit and the memory unit for receiving data items from either of those units for transfer to the other of those units, and for transferring data items with memory external to the processing element, and for storing data items for processing by the processor unit, and

wherein the controller is operable to retrieve an offset value from the storage registers, to combine the offset value with a predetermined reference address to give a calculated internal address, to retrieve external address data stored at the calculated internal address in the internal memory, and to access the external memory at the external address.

16. A data processing apparatus as claimed in claim 15, wherein the controller is operable to retrieve a stored data or instruction item from the external address in the external memory, and to transfer the retrieved data or instruction item to the processing element.

17. A data processing apparatus as claimed in claim 15, wherein the controller is operable to transfer a data item from the processing element to the external memory, for storage therein at the external memory address.

18. A data processing apparatus as claimed in any one of the preceding claims, wherein each processing element comprises:

a processor unit for processing data items in accordance with instruction items; and

an enable register for indicating whether the element is available for processing data items,

the enable register including a plurality of indicators, each operable to indicate an enabled or disabled condition of the processing element, the processing element being available for processing of data items when all said indicator units indicate the enabled condition.

19. A data processing apparatus as claimed in claim 18, wherein each indicator of the enable register is operable to indicate the status of a conditional processing step for the processing

element concerned.

20. A data processing apparatus as claimed in claim 18 or 19, wherein the enable register is provided by a hardware register.

21. A data processing apparatus as claimed in any one of the preceding claims, wherein each processing element in the array is operable to transfer data items directly with at least one neighbouring processing element, and wherein each processing block includes a processing element which is operable to transfer data items directly with a processing element in another processing block.

22. A data processing apparatus as claimed in claim 21, wherein each processing element comprises a processor unit for receiving data items and instruction items and operable to process received data items in accordance with received instruction items, a memory unit for storing data items, and a register file for storing data items and connected for transferring data items with the processor unit and with the memory unit, the register file being connected for transferring data items with memory external to the processing element, and being connected for transferring data items with neighbouring processing elements.

23. A data processing apparatus as claimed in claim 21 or 22, wherein the processing elements are

provided on a single integrated circuit.

24. A data processing apparatus as claimed in claim 23, wherein the processing elements in each processing block are connected in respective series in the integrated circuit, each processing element, except the first in the series, being operable to transfer data items directly with the previous element in the series and each processing element, except the last in the series, being operable to transfer data items directly with the next processing element in the series.

25. A data processing apparatus as claimed in claim 23, wherein the processing elements in the processing blocks are connected in respective two dimensional arrays in the integrated circuit, each processing element being operable to transfer data items with at least three neighbouring elements in the array.

26. A data processing apparatus as claimed in claim 24 or 25, wherein the processing blocks are connected in a series, the last processing element of a processing block, being operable to transfer data with the first processing element in another processing block in the series.

27. A data processing apparatus as claimed in claim 24 or 25, wherein the processing blocks are connected in a series, the last processing element of a

processing block, except the last processing block in the series, being operable to transfer data with the first processing element in the next processing block in the series.

28. A data processing apparatus as claimed in any one of the preceding claims, comprising a controller which includes:

means for retrieving instruction items for each of a plurality of instruction streams;

means for combining the plurality of instruction streams into a serial instruction stream; and,

means for distributing the serial instruction stream to either a processing controller which controls data processing of the array of processing elements, or a data transfer controller which controls the transfer of data to and from the processing elements.

29. A data processing apparatus as claimed in claim 28, comprising a cache memory for storing retrieved instruction items.

30. A data processing apparatus as claimed in claim 28 or 29, comprising:

a plurality of instruction stream processors, one for each instruction stream, for

controlling the respective instruction streams;

a semaphore controller for controlling synchronisation between instruction steams;

a status block for providing status information regarding each of the instruction streams; and

a scheduling means connected to receive status information, and operable to determine which of the instruction streams is to be active.

31. A data processing apparatus as claimed in claim 28, 29 or 30, wherein each instruction stream is assigned a relative priority level.

32. A data processing apparatus as claimed in any one of the preceding claims, comprising a semaphore controller which includes:

means for maintaining synchronism between the execution of the plurality of separate instruction streams.

33. A data processing apparatus as claimed in claim 32, having means for presetting a semaphore value.

34. A data processing apparatus as claimed in claim 32 or 33, having means for decrementing a semaphore value.

35. A data processing apparatus as claimed in any one of claims 32 to 34, having means for incrementing a semaphore value.

36. A data processing apparatus as claimed in any one of claims 32 to 35, having means for arranging the semaphores into a plurality of groups.

37. A data processing apparatus as claimed in claim 36, wherein the means for arranging the semaphores into groups is controlled according to which execution units the semaphores can be incremented.

38. A data processing apparatus as claimed in any one of claims 32 to 37, having means for controlling the access of a plurality of instruction streams to a shared resource.

39. A data processing apparatus as claimed in any one of claims 32 to 38, having means for incrementing and/or decrementing semaphore values in response to instructions issued by a processor.

40. A data processing apparatus as claimed in any one of the preceding claims, comprising an array controller which includes means connected to receive instructions, and routing means operable to transfer received instructions to the array of processing elements in dependence upon the

instruction concerned.

41. A data processing apparatus as claimed in claim 40, wherein the array controller comprises an instruction launcher for separating received instructions into data processing instructions and data transfer instructions.

42. A data processing apparatus as claimed in claim 40 or 41, wherein the routing means comprises:

a processing element instruction sequencer for handling data processing instructions which relate to processing of data by the processing elements; and

a data transfer controller for handling data transfer instructions which relate to the transfer of data items to and/or from the processing elements.

43. A data processing apparatus as claimed in claim 42, wherein the processing element instruction sequencer is operable to transfer microcode instructions to the array of processing elements, which microcode instructions relate to data processing functions of the array.

44. A data processing apparatus as claimed in claim 40, 41, 42 or 43, wherein each processing element further comprises a set of registers, and wherein

the instruction launcher includes means for determining which registers of the processing elements are accessed by an instruction, and means for preventing other instructions from accessing these registers while the instruction is being performed.

45. A data processing apparatus as claimed in claim 44, wherein the instruction launcher has means for releasing the registers for use by other instructions once the instruction has completed.

46. A data processing apparatus as claimed in any one of claims 40 to 45, further comprising an instruction table for assisting the instruction launcher in determining which registers are accessed by data processing instructions.

47. A data processing apparatus as claimed in any one of claims 40 to 46, wherein the instruction launcher maintains the appearance of serial execution, while also maintaining parallel operation between the processing element instruction sequencer and the data transfer controller.

48. A data processing apparatus as claimed in claim 47, wherein the routing means includes a register use monitor means operable to record which of the processor unit registers are in use by an instruction.

49. A data processing apparatus as claimed in claim 48, wherein the register use monitor means is operable to prevent operation of a further instruction that requires use of registers that are already in use by an instruction.

50. A data processing apparatus as claimed in any one of claims 40 to 49, wherein the data transfer controller comprises control means operable to control transfer of data to and/or from an internal memory unit of a processing element in a SIMD (single instruction multiple data) array of processing elements, each processing element including a processing unit and an internal memory unit, the control means being operable such that data transfer to and/or from the internal memory unit is performed independently of the operation of the processing unit of the processing element concerned.

51. A data processing apparatus as claimed in claim 50, wherein each processing element includes a register file for storing data items for transfer between the processor unit and the internal memory unit and for processing by the processor unit, and wherein the data transfer controller further comprises means for controlling transfer of data items between the internal memory unit and the register file of a processing element.

52. A data processing apparatus as claimed in claim 50

or 51, further comprising a mathematical expression evaluator (MEE), and wherein the data transfer controller has means for controlling transfer of data between the internal memory unit of a processing element and the expression evaluator.

53. A data processing apparatus as claimed in claim 50, 51, or 52, wherein the data transfer controller has means for transferring data between the internal memory unit of one processing element and the internal memory unit of another processing element.

54. A data processing apparatus as claimed in any one of claims 50 to 53, wherein the data transfer controller has means for performing a memory refresh on the internal memory units of the processing elements.

55. A data processing apparatus as claimed in any one of claims 50 to 55, wherein the data transfer controller has means for performing transfer of data between an internal memory unit of a processing element and memory external to the processing element.

56. A data processing apparatus as claimed in any one of the preceding claims, comprising:

a local memory unit for storing data items for transfer to and from the processing elements, the data items being stored at addresses in the memory unit; and

a segment register for each processing block, for storing segment information relating to the local memory unit, the segment information indicating the address area of the local memory unit to be accessed by the processing block concerned.

57. A data processing apparatus as claimed in claim 56, wherein the processing elements are connected to receive an instruction item which includes address information relating to the local memory unit, and are operable to access the local memory unit on the basis of the received address information and stored segment information.

58. A data processing apparatus as claimed in claim 57, wherein the processing element is operable to add the segment information to the address information to give a local memory unit target address.

59. A method of processing data using data processing apparatus as claimed in any one of the preceding claims and a local memory unit for storing data items at addresses in the local memory unit, the method comprising:

supplying an instruction item to the processing elements, the instruction item including address information relating to data items stored in the local memory unit;

obtaining segment information for each processing block, the segment information relating to the address area of the local memory unit to which a processing block has access;

combining the segment and address information to produce target address information; and

accessing the local memory unit on the basis of the target address information.

60. A data processing apparatus as claimed in any one of the preceding claims, wherein each processing element comprises a processor unit, a memory input/output port for transferring data items to and from a data storage unit, and a set of data registers for transferring data items to the processor unit, wherein each of the registers in the set of data registers is connected for receiving data items from the memory input/output port, and for receiving data items from an output of the processor unit, and for transferring data items to an input of the processor unit.

61. A data processing apparatus as claimed in claim

60, wherein the said set of data registers includes four such data registers.

62. A data processing apparatus as claimed in claim 60 or 61, comprising a data shifter connected to receive input data items from three of the said data registers, and operable to shift received data items by a predetermined number of data bits, and to transfer shifted data items to the three data registers.

63. A data processing apparatus as claimed in claim 62, wherein the data shifter receives data items from the three data registers for floating point calculations, the fourth data register being used to store the exponent of a floating point operation.

64. A data processing apparatus as claimed in claim 60, 61, 62 or 63, wherein the processing unit comprises an arithmetic logic unit.

65. A data processing apparatus as claimed in claim 60, wherein the said set of data registers includes N such data registers, where N is at least four.

66. A data processing apparatus as claimed in claim 65, comprising a data shifter connected to receive input data items from N-1 of the said data

registers, and operable to shift received data items by a predetermined number of data bits, and to transfer shifted data items to the N-1 data registers.

67. A data processing apparatus as claimed in claim 66, wherein the data shifter receives data items from the N-1 data registers for floating point calculations, the Nth data register being used to store the exponent of a floating point operation.

68. A method of scheduling instruction streams in a data processing apparatus as claimed in any one of the preceding claims, the method comprising determining which instruction stream has priority at a particular moment in time, and transferring that instruction stream to the SIMD array.

69. A method as claimed in claim 68, comprising the steps of:

determining whether an instruction stream with higher priority that the currently active stream is ready to execute; and,

if a higher priority instruction stream is ready to execute, activating the instruction stream having the higher priority.

70. A method as claimed in claim 68, comprising

the steps of:

determining whether an active instruction stream has stalled; and,

if a higher priority instruction stream is pending, activating the instruction stream having the higher priority.

71. A method of controlling data read access to memory in a data processing apparatus as claimed in any one of claims 1 to 67, the method comprising:

selecting a processing element that requires access to the memory,

retrieving a target address from the selected processing element,

transmitting the target address to the plurality of processing elements,

transmitting transaction identification information to the processing elements, which information identifies the target address access operation concerned,

storing the transaction identification information in the or each processing element that requires access to the target address,

transmitting data obtained from the target address together with the transaction identification information to the plurality of processing elements, and

storing the obtained data in the or each processing element in which the transaction identification information is stored.

72. A method of retrieving a data item from a memory unit in a data processing apparatus as claimed in any one of claims 1 to 67, and which includes a memory unit in which data items are stored at addresses therein, and a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target

address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the or each retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the or each retrieved data item.

73. A method of writing data items to a memory unit in a data processing apparatus as claimed in any one of claims 1 to 67 including the memory unit in which data items are stored at addresses therein, and a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which

requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information

with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the or each transmitted data item at the target address in the memory unit.

74. A method as claimed in claim 73, wherein processing elements store data items at respective regions of the target memory address.

75. A method of controlling a plurality of instruction streams operating in a data processing apparatus as claimed in any one of claims 1 to 67, the method comprising:

providing a plurality of semaphore values which serve to indicate the status of respective resources within the data processing apparatus; and

controlling operation of the instruction streams in dependence upon the semaphore values.

76. A method as claimed in claim 75, wherein controlling operation of an instruction stream comprises:

evaluating the semaphore value for a resource; and

if the evaluated semaphore value equals a predetermined value, halting operation of the instruction stream, or

if the evaluated semaphore value is greater than the predetermined value, decrementing the semaphore value and continuing operation of the instruction stream.

77. A method as claimed in claim 75, wherein controlling operation of an instruction stream comprises:

evaluating the semaphore value for a resource; and

if the evaluated semaphore value equals a predetermined value, halting operation of the instruction stream, or

if the evaluated semaphore value is less than the predetermined value, incrementing the semaphore value and continuing operation of the instruction stream.

78. A method as claimed in claim 75, 76 or 77, wherein

a negative semaphore value indicates the number of instruction streams that have been paused by that particular semaphore value.

79. A method as claimed in any one of claims 75 to 78, wherein each semaphore value can be incremented by an instruction stream, or by an execution unit in the SIMD array.

80. A method as claimed in any one of claims 75 to 78, wherein the semaphores are arranged in a plurality of groups.

81. A method as claimed in claim 80, wherein the semaphore groups are arranged according to which execution units the semaphores can be incremented.

82. A method as claimed in any one of claims 75 to 81, wherein a predetermined semaphore is used to control the access of a plurality of instruction streams to a shared resource.

83. A method as claimed in any one of claims 75 to 82, wherein semaphore values may be incremented and/or decremented by a processor.

84. A data processing apparatus as claimed in any one of claims 1 to 67, provided on a single integrated circuit.

85. A monolithic integrated circuit comprising a central processing unit and a data processing apparatus as claimed in any one of claims 1 to 67.

86. A graphical data processing system comprising a host general data processing apparatus and a data processing apparatus as claimed in any one of claims 1 to 67 for processing graphical data.

87. A system as claimed in claim 86 provided on a single integrated circuit.

88. A data processing apparatus comprising a plurality of processing elements, operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items.

89. A data processing apparatus substantially as hereinbefore described with reference to, and as shown in, the accompanying drawings.

90. A method of processing data items using a SIMD (single instruction multiple data) array of processing elements, the method comprising:

supplying a common instruction to all of the processing elements in the array; and

supplying respective data items to the processing elements such that each processing element processes a different data item in accordance with the common instruction,

wherein the data items are supplied to the processing elements independently from the instruction item.

91. A method as claimed in claim 90, wherein the data items to be processed by the array are supplied directly by at least one of the processing elements in the array.

92 A method as claimed in claim 90, wherein the processing elements are operably divided into a plurality of processing blocks, each block being operable to process data items from a predetermined group

93. A method of processing data items using a SIMD (single instruction multiple data) array of processing elements, and a mathematical expression evaluator which is operable to produce an evaluation of mathematical expression for each processing element in the array in accordance with instructions and coefficients received by the evaluator, the method comprising:

supplying a stream of instruction items to

the evaluator; and

supplying at least one coefficient to the evaluator,

wherein the or each coefficient is supplied to the evaluator independently from the instruction items.

94. A method as claimed in claim 93, wherein the or each coefficient is supplied by at least one of the processing elements in the array.

95. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements which are connected to receive a common instruction item and respective data items, wherein the data items and the instruction item are supplied independently of one another to the processing elements.

96. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements which are connected to receive a common instruction item and respective data items, and a mathematical expression evaluator connected to receive instruction items and coefficient data items, and operable to evaluate a mathematical expression for each processing element, and to supply respective evaluations to

the processing elements, wherein the coefficient data items and the instruction items are supplied independently of one another to the mathematical expression evaluator.

97. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements in which the processing elements are operably divided into a plurality of active processing blocks, the processing blocks being operable to process respective groups of data items, wherein at least one of the processing blocks is a redundant block operable to process a group of data items in place of a faulty processing block.

98. An apparatus as claimed in claim 97, comprising fault detection means operable to detect a fault occurring in a processing block and to transfer the data processing function of that processing block to a redundant processing block.

99. An apparatus as claimed in claim 97 or 98, wherein each processing block is provided with at least one redundant processing element operable to process data items in place of a faulty processing element of the block concerned.

100. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements in which the processing

elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, wherein each processing block is provided with at least one redundant processing element operable to process data items in place of a faulty processing element of the block concerned.

101. An apparatus as claimed in claim 99 or 100, wherein the processing elements of a processing block are arranged in groups having a predetermined number of processing elements therein, each such group containing at least one such redundant processing element for replacing a faulty processing element in the group.

102. An apparatus as claimed in claim 99, 100 or 101, comprising fault detection means operable to detect a fault occurring in a processing element and to transfer the data processing function of that processing element to a redundant processing element.

103. A data processing apparatus comprising:

a single instruction multiple data (SIMD) array of processing elements for processing data items in accordance with instruction items, the array of processing elements being operably divided into a plurality of processing blocks operable to process respective groups of data items;

a local memory unit for storing data items for transfer to and from the processing elements, the data items being stored at addresses in the memory unit; and

a segment register for each processing block, for storing segment information relating to the local memory unit, the segment information indicating the address area of the local memory unit to be accessed by the processing block concerned.

103. A data processing apparatus comprising:

a single instruction multiple data (SIMD) array of processing elements for processing data items in accordance with instruction items, the array of processing elements being operably divided into a plurality of processing blocks operable to process respective groups of data items;

a local memory unit for storing data items for transfer to and from the processing elements, the data items being stored at addresses in the memory unit; and

a segment register for each processing block, for storing segment information relating to the local memory unit, the segment information indicating the address area of the local memory unit to be accessed by the processing block concerned.

104. A data processing apparatus as claimed in claim 103, wherein the processing elements are connected to receive an instruction item which includes address information relating to the local memory unit, and are operable to access the local memory unit on the basis of the received address information and stored segment information.

105. A data processing apparatus as claimed in claim 104, wherein the processing element is operable to add the segment information to the address information to give a local memory unit target address.

106. A method of processing data using data processing apparatus which includes a single instruction multiple data (SIMD) array of processing elements, the array of processing elements being operably divided into a plurality of processing blocks operable to process respective groups of data items, and a local memory unit for storing data items for transfer to and from the processing elements, the data items being stored at addresses in the local memory unit, the method comprising:

supplying an instruction item to the processing elements, the instruction item including address information relating to data items stored in the local memory unit;

obtaining segment information for each processing

block, the segment information relating to the address area of the local memory unit to which a processing block has access;

combining the segment and address information to produce target address information; and

accessing the local memory unit on the basis of the target address information.

107. A method as claimed in claim 106, wherein the segment and address information are combined by adding the segment information to the address information.

108. A method of processing data items using a SIMD (single instruction multiple data) array of processing elements, the method comprising:

supplying a common instruction to all of the processing elements in the array; and

supplying respective data items to the processing elements such that each processing element processes a different data item in accordance with the common instruction,

wherein the instruction is supplied to the processing elements separately from the data

items, and wherein the data items are supplied by at least one of the processing elements in the array.

109. A method of processing data items using a SIMD (single instruction multiple data) array of processing elements, the method comprising:

supplying a common instruction to all of the processing elements in the array;

evaluating a mathematical expression for each processing element in the array to produce result data item for each processing element; and

supplying respective result data items to the processing elements,

wherein the instruction is supplied to the processing elements separately from the result data items, and wherein coefficients for the mathematical expression are supplied by at least one of the processing elements in the array.

110. A method as claimed in claim 108 or 109, wherein the processing elements are operably divided into a plurality of processing blocks, each block being operable to process data items from a predetermined group of data items.

111. A data processing apparatus comprising:

a plurality of processing elements operable to process respective data items in accordance with a common instruction, the processing element thereby forming a single instruction multiple data (SIMD) array of processing elements;

control means operable to supply instructions to the processing elements;

operand supply means operable to supply data items to the processing elements for processing thereby in accordance with instructions received by the processing elements,

wherein the operand supply means is connected to receive data items for supply to the processing elements from at least one of the processing elements in the array.

112. A data processing architecture comprising:

a plurality of processing elements operable to process respective data items in accordance with a common instruction, the processing element thereby forming a single instruction multiple data (SIMD) array of processing elements;

control means operable to supply instructions to the processing elements;

a mathematical expression evaluator operable to evaluate a mathematical expression for each processing element in the array; and

operand supply means operable to supply coefficients to the evaluator for processing thereby,

wherein the operand supply means is connected to receive coefficients for supply to the evaluator from at least one of the processing elements in the array.

113. A method of controlling access to an external memory by a processing element including an internal memory in which a target external memory address is stored at an internal address therein, which internal address is offset from a reference address by an offset value, the target address indicating the address in the external memory to which access is required, the method comprising:

retrieving the offset value;

combining the reference address and the offset value to produce a calculated internal

address;

retrieving the target address from the internal memory at the address therein given by the calculated internal address; and

accessing the external memory on the basis of the retrieved target address.

114. A method as claimed in claim 113, wherein the processing element comprises a processor unit for processing data items in accordance with received instructions, the processor unit including a register for storing data items for transfer to the processor unit, and for storing the said offset value.

115. A method as claimed in claim 113 or 114, wherein accessing the external memory comprises retrieving a stored data or instruction item from the target address in external memory and transferring the retrieved data or instruction item to the processing element.

116. A method as claimed in claim 113, 114 or 115, wherein accessing the external memory comprises supplying data items to the external memory for storage therein at the target address.

117. A data processing apparatus comprising:

at least one processing element for processing data items in accordance with instruction items;

an external memory for storing data items and instruction items; and

a controller means for controlling transfer of data and instruction items between the or each processing element and the memory,

wherein the or each processing element comprises:

a processor unit connected to receive data items and instruction items and operable to process the said data items in accordance with the said instruction items;

a plurality of storage registers for temporarily storing data items for input to the processor unit, at least one of the storage registers being operable to store an offset value;

a memory unit for storing data items and address data indicating an external memory address; and

a register file for storing data items, the

register file being connected between the processor unit and the memory unit for receiving data items from either of those units for transfer to the other of those units, and for transferring data items with memory external to the processing element, and for storing data items for processing by the processor unit, and

wherein the controller is operable to retrieve an offset value from the storage registers, to combine the offset value with a predetermined reference address to give a calculated internal address, to retrieve external address data stored at the calculated internal address in the internal memory, and to access the external memory at the external address.

118. A data processing apparatus as claimed in claim 117, wherein the controller is operable to retrieve a stored data or instruction item from the external address in the external memory, and to transfer the retrieved data or instruction item to the processing element.

119. A data processing apparatus as claimed in claim 117, wherein the controller is operable to transfer a data item from the processing element to the external memory, for storage therein at the external memory address.

120. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein each processing element comprises:

a processor unit for processing data items in accordance with instruction items; and

an enable register for indicating whether the element is available for processing data items,

the enable register including a plurality of indicators, each operable to indicate an enabled or disabled condition of the processing element, the processing element being available for processing of data items when all said indicator units indicate the enabled condition.

121. A data processing apparatus as claimed in claim 120, wherein each indicator of the enable register is operable to indicate the status of a conditional processing step for the processing element concerned.

122. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein each processing element comprises a processor unit, a memory input/output port for transferring data items to and from a data storage unit, and a set of data

registers for transferring data items to the processor unit, wherein each of the registers in the set of data registers is connected for receiving data items from the memory input/output port, and for receiving data items from an output of the processor unit, and for transferring data items to an input of the processor unit.

123. A data processing apparatus as claimed in claim 122, wherein the said set of data registers includes four such data registers.

124. A data processing apparatus as claimed in claim 122 or 123 comprising a data shifter connected to receive input data items from three of the said data registers, and operable to shift received data items by a predetermined number of data bits, and to transfer shifted data items to the three data registers.

125. A data processing apparatus as claimed in claim 124, wherein the data shifter receives data items from the three data registers for floating point calculations, the fourth data register being used to store the exponent of a floating point operation.

126. A data processing apparatus as claimed in any one of claims 122 to 125, wherein the processing unit comprises an arithmetic logic unit.

127. A data processing apparatus as claimed in claim 122, wherein the said set of data registers includes N such data registers, where N is at least four.

128. A data processing apparatus as claimed in claim 128, comprising a data shifter connected to receive input data items from N-1 of the said data registers, and operable to shift received data items by a predetermined number of data bits, and to transfer shifted data items to the N-1 data registers.

129. A data processing apparatus as claimed in claim 129, wherein the data shifter receives data items from the N-1 data registers for floating point calculations, the Nth data register being used to store the exponent of a floating point operation.

130. A data processing apparatus comprising a SIMD (single instruction multiple access) array of processing elements, wherein each processing element comprises a processor unit for receiving data items and instruction items and operable to process received data items in accordance with received instruction items, a memory unit for storing data items, and a register file for storing data items and connected for transferring data items with the processor unit and with the memory unit, the register file also being connected for transferring data items with memory

external to the processing element, and operable to store data items for processing by the processor unit of the processing element.

131. A data processing apparatus as claimed in claim 130, wherein each processor unit is operable to store a data item in the register file and simultaneously to read a data item from the register file.

132. A data processing apparatus as claimed in claim 130 or 131, wherein each memory unit is provided by a dynamic random access memory (DRAM) unit.

133. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements in which the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, wherein each processing element in the array is operable to transfer data items directly with at least one neighbouring processing element, and wherein each processing block includes a processing element which is operable to transfer data items directly with a processing element in another processing block.

134. A data processing apparatus as claimed in claim 133, wherein each processing element comprises a

processor unit for receiving data items and instruction items and operable to process received data items in accordance with received instruction items, a memory unit for storing data items, and a register file for storing data items and connected for transferring data items with the processor unit and with the memory unit, the register file being connected for transferring data items with memory external to the processing element, and being connected for transferring data items with neighbouring processing elements.

135. A data processing apparatus as claimed in claim 133 or 134, wherein the processing elements are provided on a single integrated circuit.

136. A data processing apparatus as claimed in claim 135, wherein the processing elements in each processing block are connected in respective series in the integrated circuit, each processing element, except the first in the series, being operable to transfer data items directly with the previous element in the series and each processing element, except the last in the series, being operable to transfer data items directly with the next processing element in the series.

137. A data processing apparatus as claimed in claim 136, wherein the processing elements in the processing blocks are connected in respective two dimensional arrays in the integrated circuit, each processing element being operable to transfer data

items with at least three neighbouring elements in the array.

138. A data processing apparatus as claimed in claim 136 or 137, wherein the processing blocks are connected in a series, the last processing element of a processing block, being operable to transfer data with the first processing element in another processing block in the series.

139. A data processing apparatus as claimed in claim 136 or 137, wherein the processing blocks are connected in a series, the last processing element of a processing block, except the last processing block in the series, being operable to transfer data with the first processing element in the next processing block in the series.

140. A controller for controlling an array of processing elements, each of which includes a processing unit and an internal memory unit, the controller comprising:

means for retrieving instruction items for each of a plurality of instruction streams;

means for combining the plurality of instruction streams into a serial instruction stream; and,

means for distributing the serial instruction stream to either a processing controller which controls data processing of

the array of processing elements, or a data transfer controller which controls the transfer of data to and from the processing elements.

141. A controller as claimed in claim 140, comprising a cache memory for storing retrieved instruction items.

142. A controller as claimed in claim 140 or 141, comprising:

a plurality of instruction stream processors, one for each instruction stream, for controlling the respective instruction streams;

a semaphore controller for controlling synchronisation between instruction steams;

a status block for providing status information regarding each of the instruction streams; and

a scheduling means connected to receive status information, and operable to determine which of the instruction streams is to be active.

143. A controller as claimed in any one of claims 140 to 142, wherein each instruction stream is assigned a relative priority level.

144. A controller as claimed in any one of claims 140 to 143, wherein the array of processors is a SIMD (single instruction multiple data) array.

145. A thread manager for use in an array of processing elements each of which includes a processing unit and an internal memory unit, the thread manager comprising:

means for retrieving instruction items from external memory for each of a plurality of threads, each thread being a stream of instructions;

means for combining the threads into a serial command stream; and,

means for distributing the serial command stream to either a processing controller which controls data processing of the array of processing elements, or a input/output data transfer channel controller which controls the transfer of data between external memory and internal memory units of the processing elements.

146. A thread manager as claimed in claim 145, comprising a cache memory for buffering the instruction retrievals from memory.

147. A thread manager as claimed in claims 145 or 146, comprising:

a plurality of thread processors, one for

each active thread, and for controlling the respective thread;

a semaphore controller for controlling synchronisation between threads; and,

a status block for providing status information regarding each of the threads.

148. A thread manager as claimed in any one of claims 145 to 147, comprising scheduler means for determining which thread should be active at any particular moment in time.

149. A thread manager as claimed in any one of claims 145 to 148, wherein the array of processors is a SIMD (single instruction multiple data) array.

150. A method of scheduling instruction streams in a SIMD (single instruction multiple data) array of processing elements, the method comprising determining which instruction stream has priority at a particular moment in time, and transferring that instruction stream to the SIMD array.

151. A method as claimed in claim 150, comprising the steps of:

determining whether an instruction stream with higher priority that the currently active stream is ready to execute; and,

if a higher priority instruction stream is ready to execute, activating the instruction stream having the higher priority.

152. A method as claimed in claim 151, comprising the steps of:

determining whether an active instruction stream has stalled; and,

if a higher priority instruction stream is pending, activating the instruction stream having the higher priority.

153. A method of controlling a plurality of instruction streams operating in a data processing apparatus including a SIMD (single instruction multiple data) array of processing elements, the method comprising:

providing a plurality of semaphore values which serve to indicate the status of respective resources within the data processing apparatus; and

controlling operation of the instruction streams in dependence upon the semaphore values.

154. A method as claimed in claim 153, wherein controlling operation of an instruction stream comprises:

evaluating the semaphore value for a resource; and

if the evaluated semaphore value equals a predetermined value, halting operation of the instruction stream, or

if the evaluated semaphore value is greater than the predetermined value, decrementing the semaphore value and continuing operation of the instruction stream.

155. A method as claimed in claim 153 or 154, wherein controlling operation of and instruction stream comprises:

evaluating the semaphore value for a resource; and

if the evaluated semaphore value equals a predetermined value, halting operation of the instruction stream, or

if the evaluated semaphore value is less than the predetermined value, incrementing the semaphore value and continuing operation of the instruction stream.

156. A method as claimed in claim 155, wherein a negative semaphore value indicates the number of instruction streams that have been paused by that particular semaphore value.

157. A method as claimed in any one of claims 153 to 156, wherein each semaphore value can be incremented by an instruction stream, or by an execution unit in the SIMD array.

158. A method as claimed in any one of claims 153 to 157, wherein the semaphores are arranged in a plurality of groups.

159. A method as claimed in claim 158, wherein the semaphore groups are arranged according to which execution units the semaphores can be incremented by.

160. A method as claimed in any one of claims 153 to 159, wherein a predetermined semaphore is used to control the access of a plurality of instruction streams to a shared resource.

161. A method as claimed in any one of claims 153 to 160, wherein semaphore values may be incremented and/or decremented by a processor.

162. A semaphore controller for use in a SIMD (single

instruction multiple data) array of processing elements in which the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, each processing element comprising a processing unit and an internal memory unit, and in which the SIMD array processes a plurality of separate instruction streams, the semaphore controller comprising:

means for maintaining synchronism between the execution of the plurality of separate instruction streams.

163. A semaphore controller as claimed in claim 162, having means for presetting a semaphore value.

164. A semaphore controller as claimed in claim 162 or 163, having means for decrementing a semaphore value.

165. A semaphore controller as claimed in any one of claims 162 to 164, having means for incrementing a semaphore value.

166. A semaphore controller as claimed in any one of claims 162 to 165, having means for arranging the semaphores into a plurality of groups.

167. A semaphore controller as claimed in claim 166,

wherein the means for arranging the semaphores into groups is controlled according to which execution units the semaphores can be incremented by.

168. A semaphore controller as claimed in any one of claims 162 to 167, having means for controlling the access of a plurality of instruction streams to a shared resource.

169. A semaphore controller as claimed in any one of claims 162 to 168, having means for incrementing and/or decrementing semaphore values in response to instructions issued by an EPU.

170. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements and a semaphore controller which includes:

means for maintaining synchronism between the execution of the plurality of separate instruction streams.

171. A data transfer controller for controlling transfer of data items in a data processing system, the controller comprising:

control means operable to control transfer of

data to and/or from an internal memory unit of a processing element in an array of processing elements, each processing element including a processing unit and an internal memory unit, the control means being operable such that data transfer to and/or from the internal memory unit is performed independently of the operation of the processing unit of the processing element concerned.

172. A data processing apparatus comprising:

an array of processing elements in which each processing element includes a processing unit for processing data items and an internal memory unit for storing data items; and

a data transfer controller operable to control transfer of data to and/or from an internal memory unit of a processing element such that data transfer to and/or from the internal memory unit is independent of the operation of the processing unit of the processing element concerned.

173. A data processing apparatus as claimed in claim 171 or 172, wherein the array of processing elements is a SIMD (single instruction multiple data) array.

174. A data processing apparatus as claimed in claim 171, 172 or 173, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items.

175. A data processing apparatus as claimed in any one of claims 171 to 174, wherein each processing element includes a register file for storing data items for transfer between the processor unit and the internal memory unit and for processing by the processor unit, and wherein the data transfer controller further comprises means for controlling transfer of data items between the internal memory unit and the register file of a processing element.

176. A data processing apparatus as claimed in claim 172, 173, 174 or 175, further comprising a mathematical expression evaluator (MEE), and wherein the data transfer controller has means for controlling transfer of data between the internal memory unit of a processing element and the expression evaluator.

177. A data processing apparatus as claimed in any one of claims 172 to 176, wherein the data transfer controller has means for transferring data between the internal memory unit of one processing element and the internal memory unit of another processing element.

178. A data processing apparatus as claimed in any one of claims 172 to 177, wherein the data transfer controller has means for performing a memory refresh on the internal memory units of the processing elements.

179. A data processing apparatus as claimed in any one of claims 172 to 178, wherein the data transfer controller has means for performing transfer of data between an internal memory unit of a processing element and memory external to the processing element.

180. A method of transferring data in a data processing system which includes an array of processing elements, each processing element including a processing unit and an internal memory unit and being operable to process data, the method comprising:

transferring data to and/or from an internal memory unit of a processing element such that data transfer to and/or from the internal memory units is performed independently of the operation of the processor unit of the processing element concerned.

181. A method of transferring data in a data processing apparatus comprising an array of processing elements in which the processing elements are operably divided into a plurality of processing

blocks, the processing blocks being operable to process respective groups of data items, wherein each processing element includes a processing unit and an internal memory unit and is operable to process data, the method comprising;

controlling the transfer of data to and/or from an internal memory unit of a processing element such that data transfer to and/or from that internal memory unit is independent of the operation of the processor unit of the processing element concerned.

182. A data processing apparatus comprising:

a SIMD (single instruction multiple data) array of processing elements operable to process data items and each comprising a processor unit, which includes a plurality of registers for storing data therein, and an internal memory unit; and

an array controller which is connected to receive instructions, and is operable to control the operation of the SIMD array in accordance with the received instructions,

wherein the array controller comprises:

an instruction launcher for separating

received instructions into data processing instructions and data transfer instructions;

a processing element instruction sequencer connected for receiving data processing instructions from the instruction launcher and for transferring data processing instructions to the processing elements, and;

a data transfer controller connected for receiving data transfer instructions from the instruction launcher and for controlling data transfer to and from the respective internal memory units of the processing elements; and

a register use monitor means operable to record which of the processor unit registers are in use by an instruction.

183. A data processing apparatus as claimed in claim 182, wherein the register use monitor means is operable to prevent operation of a further instruction that requires use of registers that are already in use by an instruction.

184. A data processing apparatus as claimed in claim 182 or 183, wherein the processing elements are operably divided into a plurality of processing blocks for processing respective groups of data items.

185. A register score-boarding unit for use in an array controller for controlling the operation of a SIMD (single instruction multiple data) array of processing elements in which the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, the array controller comprising a processing element instruction sequencer for handling data processing instructions and a data transfer controller for handling data transfer instructions, the register score-boarding unit comprising:

means for maintaining the appearance of serial instruction execution while achieving parallel operation between the processing element instruction sequencer and the data transfer controller.

186. An array controller for controlling operation of an array of processing elements, the controller comprising means connected to receive instructions, and routing means operable to transfer received instructions to the array of processing elements in dependence upon the instruction concerned.

187. A controller as claimed in claim 186, comprising means for separating received instructions into data processing instructions and data transfer instructions.

188. A controller as claimed in claim 185 or 186, wherein the routing means comprises:

a processing element instruction sequencer for handling data processing instructions which relate to processing of data by the processing elements; and

a data transfer controller for handling data transfer instructions which relate to the transfer of data items to and/or from the processing elements.

189. A controller as claimed in claim 188, wherein the processing element instruction sequencer is operable to transfer microcode instructions to the array of processing elements, which microcode instructions relate to data processing functions of the array.

190. A data processing apparatus comprising:

an array of processing elements each of which includes a processing unit and an internal memory unit and is operable to process data; and,

an array controller which comprises means connected to receive instructions, and routing means operable to transfer received instructions to the array of processing elements in dependence upon the instruction concerned.

191. A data processing apparatus as claimed in claim 190, wherein the array controller comprises an instruction launcher for separating received instructions into data processing instructions and data transfer instructions.

192. A data processing apparatus as claimed in claim 190 or 191, wherein the routing means comprises:

a processing element instruction sequencer for handling data processing instructions which relate to processing of data by the processing elements; and

a data transfer controller for handling data transfer instructions which relate to the transfer of data items to and/or from the processing elements.

193. A data processing apparatus as claimed in claim 192, wherein the processing element instruction sequencer is operable to transfer microcode instructions to the array of processing elements, which microcode instructions relate to data processing functions of the array.

194. A data processing apparatus as claimed in any one of claims 190 to 193, wherein each processing element further comprises a set of registers, and wherein the instruction launcher includes means for determining which registers of the processing elements are accessed by an instruction, and means

for preventing other instructions from accessing these registers while the instruction is being performed.

195. A data processing apparatus as claimed in claim 194, wherein the instruction launcher has means for releasing the registers for use by other instructions once the instruction has completed.

196. A data processing apparatus as claimed in any one of claims 190 to 194, further comprising an instruction table for assisting the instruction launcher in determining which registers are accessed by data processing instructions.

197. A data processing apparatus as claimed in any one of claims 190 to 196, wherein the instruction launcher maintains the appearance of serial execution, while also maintaining parallel operation between the processing element instruction sequencer and the data transfer controller.

198. A data processing apparatus as claimed in claim 197, wherein the routing means includes a register use monitor means operable to record which of the processor unit registers are in use by an instruction.

199. A method of controlling data read access to memory

in a data processing apparatus including a plurality of processing elements, the method comprising:

selecting a processing element that requires access to the memory,

retrieving a target address from the selected processing element,

transmitting the target address to the plurality of processing elements,

transmitting transaction identification information to the processing elements, which information identifies the target address access operation concerned,

storing the transaction identification information in the or each processing element that requires access to the target address,

transmitting data obtained from the target address together with the transaction identification information to the plurality of processing elements, and

storing the obtained data in the or each processing element in which the transaction identification information is stored.

200. A method of retrieving a data item from a memory unit in a data processing apparatus which includes a memory unit in which data items are stored at addresses therein, and a plurality of processing elements which have access to the memory unit, the

method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the or each retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the or each retrieved data item.

201. A method as claimed in claim 199 or 200, wherein the required data is returned in the order in which the transaction identification information is produced.

202. A method as claimed in claim 199 or 200, wherein the required data is returned in the order in which it is retrieved from the memory.

203. A method of writing data items to a memory unit in a data processing apparatus including the memory unit in which data items are stored at addresses therein, and a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which

requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information

with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the or each transmitted data item at the target address in the memory unit.

204. A method as claimed in claim 203, wherein processing elements store data items at respective regions of the target memory address.

205. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, data storage means for storing data items for access by the processing elements, and control means for controlling access to the storage means in accordance with a method as claimed in any one of claims 199 to 204.